

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Darren L. Anand, et al.

Examiner: James C. Kerveros

Serial No: 10/707,071

Art Unit: 2117

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Docket: BUR920030168US1 (17124)

For: AUTOMATIC BIT FAIL MAPPING FOR
EMBEDDED MEMORIES WITH CLOCK
MULTIPLIERS

Date: April 11, 2008

Confirmation No: 1070

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT

Sir:

In response to the Office Action dated January 11, 2008, applicants submit the following amendments and remarks for consideration by the Examiner and entry of record in the above-identified patent application.

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks begin on page 9 of this paper.

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being deposited with the United States Patent & Trademark Office via Electronic Filing through the United States Patent and Trademark Office e-business website, on the date shown below.

Dated: April 11, 2008


Steven Fischman